



MS-7599

CPU

VER:4.0

AMD M3 Phenom/Athlon 64 FX AM3

System Chipset

AMD RX780/RX880

ATI SB810/850

On Board Chip

FINTEK Super I/O -- F71889ED

LAN -- RTL8111DL

HD Codec --ALC892

BIOS -- SPI ROM 8M

Main Memory

DDR III X 4 (Max 8GB)

Expansion Slots

PCI-E X 16*1

PCI-E X 4 *1

PCI-E X 1 *1

PCI 2.2 Slot X 3

PWM

Controller--Intersil ISL6323 4+1 Phase

Vcore 4 Phase (MOS HIGHX2 LOWX2)

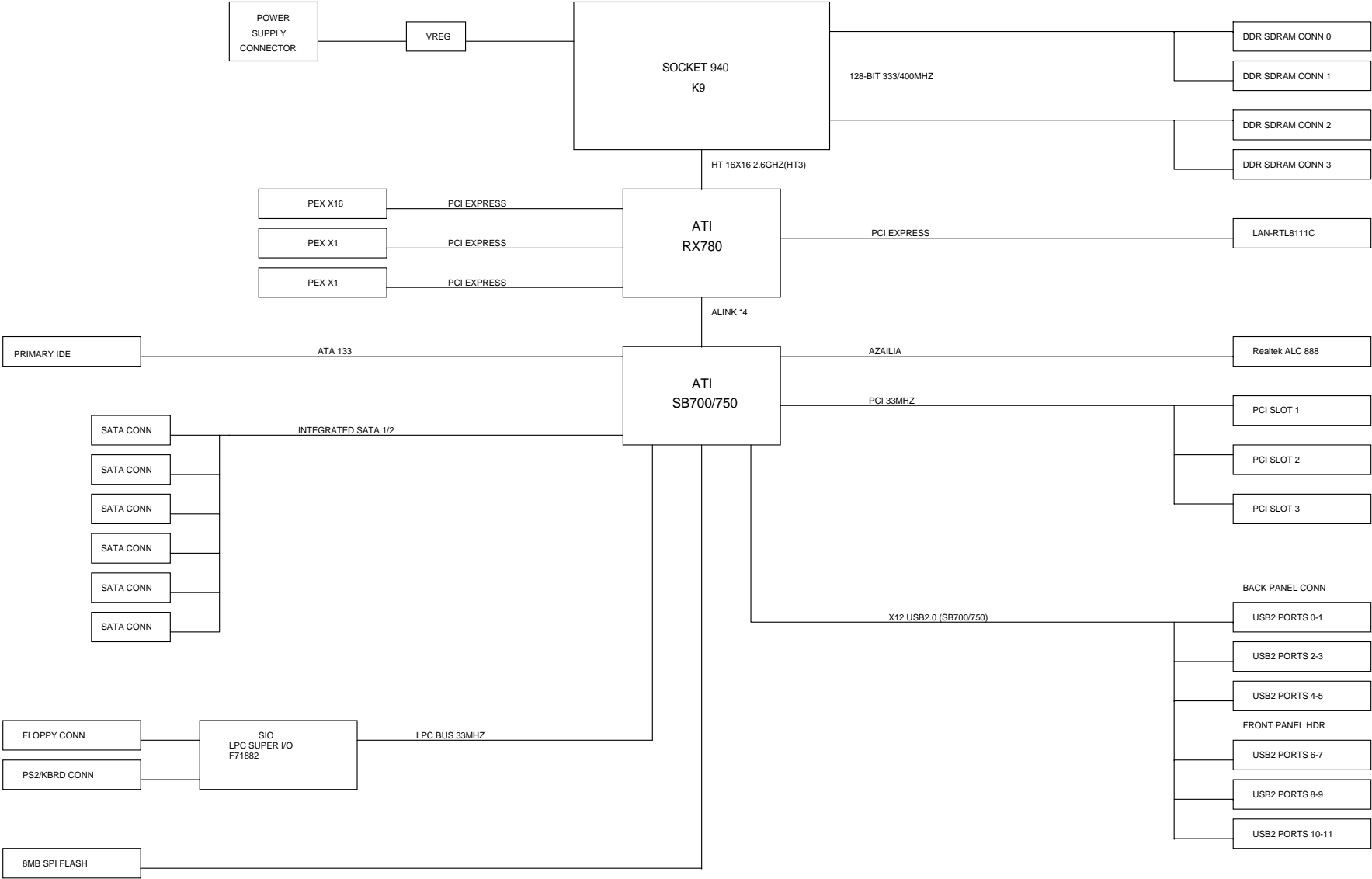
Vnb 1 Phase (MOS HIGHX1 LOWX2)

Clock Generator

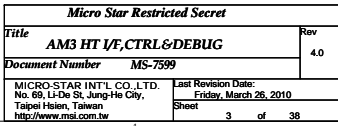
Controller--RTM880N-793

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BLOCK DIAGRAM

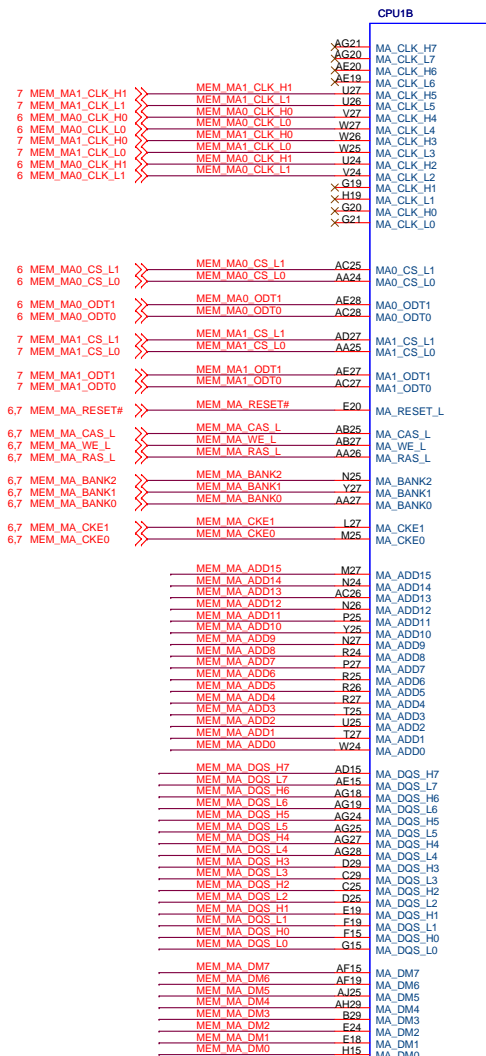


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Title	Block Diagram	Rev
Document Number	MS-7599	4.0
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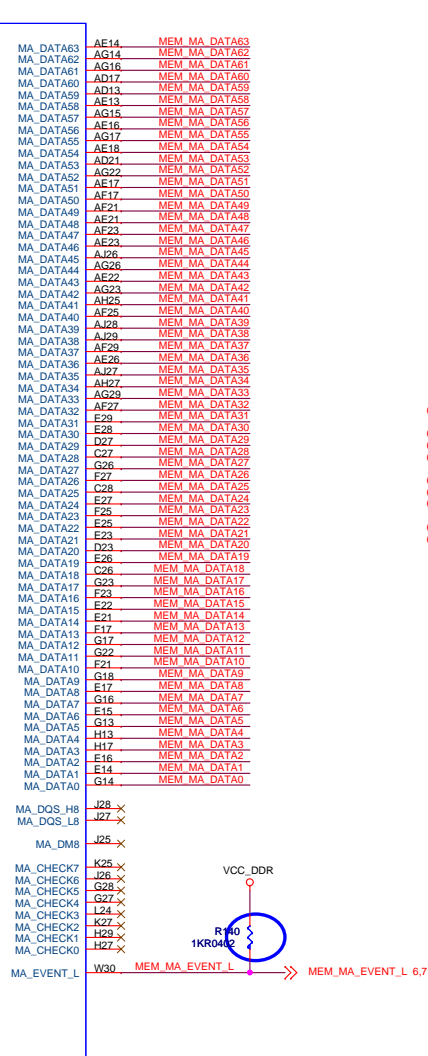


6,7 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
6,7 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
6,7 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
6,7 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
6,7 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

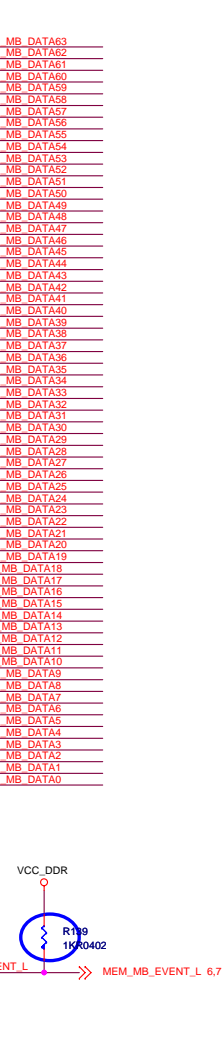
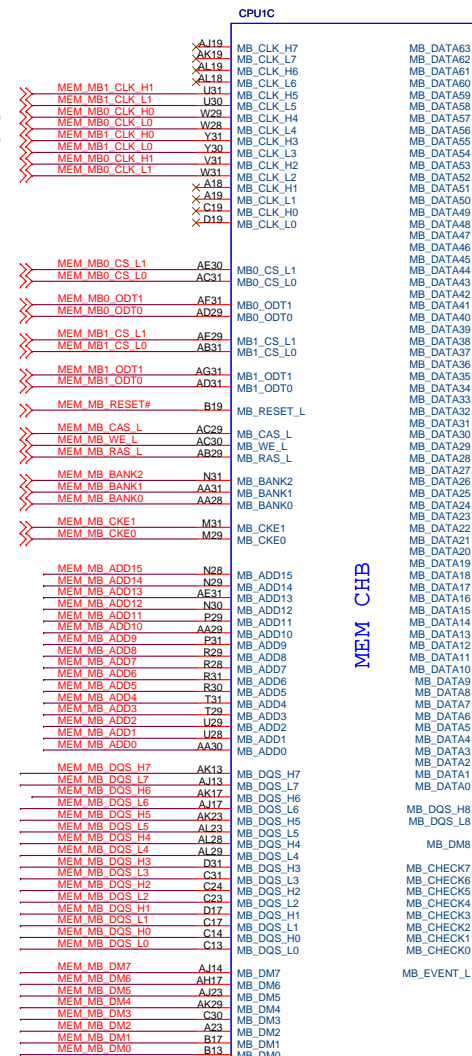
6,7 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
6,7 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
6,7 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
6,7 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
6,7 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]



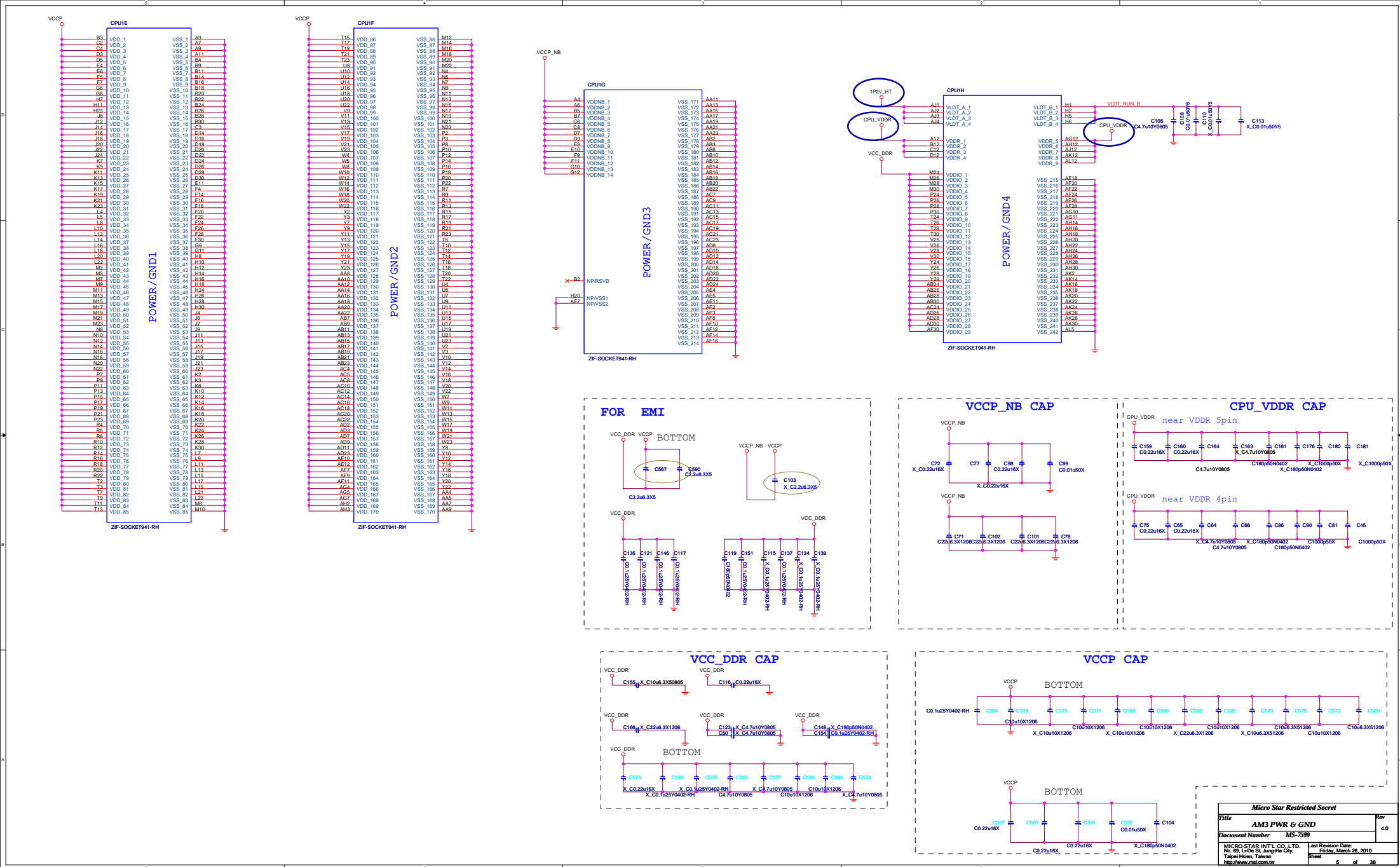
ZIF-SOCKET941-RH



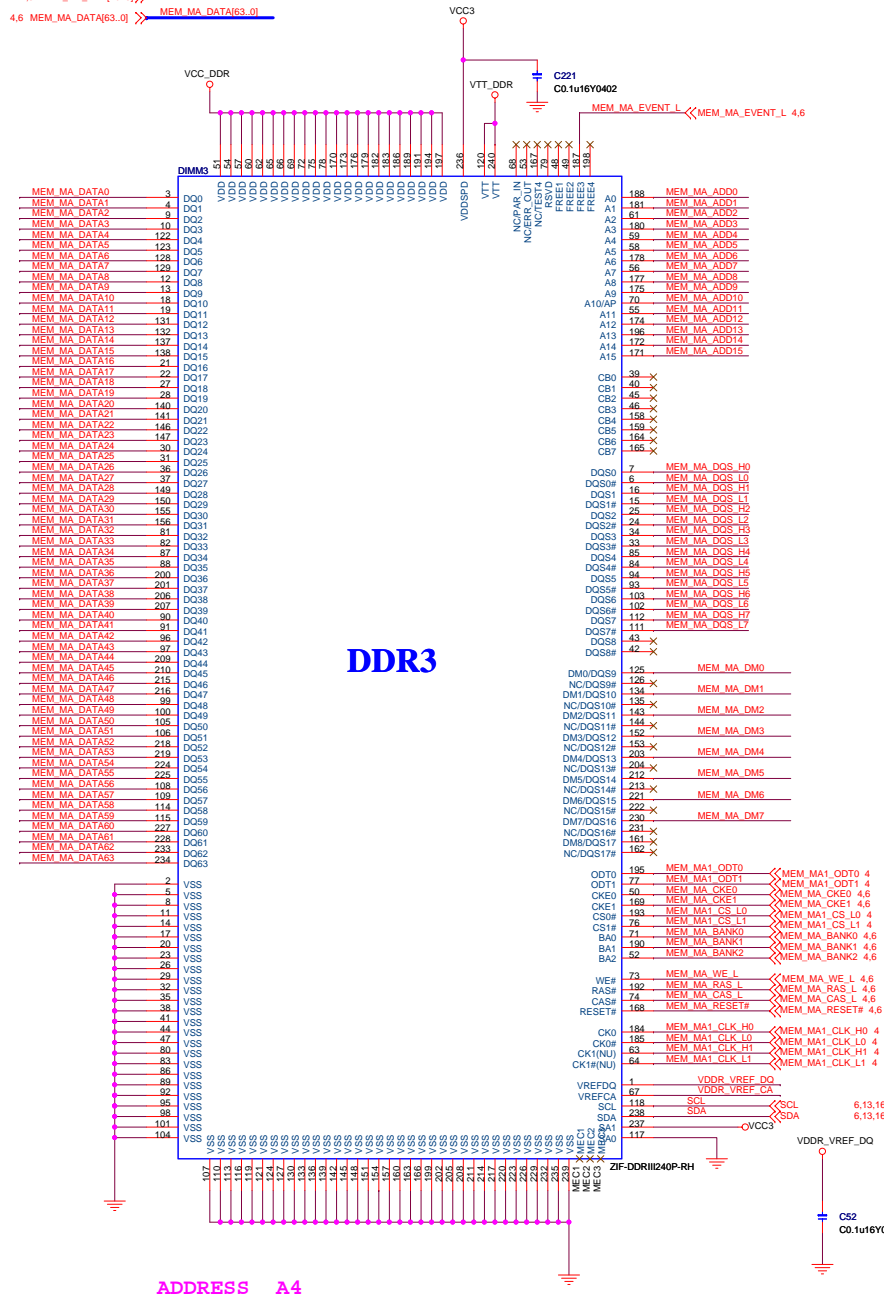
MEM MA EVENT_L 6.7



MEM MB EVENT_L 6.7

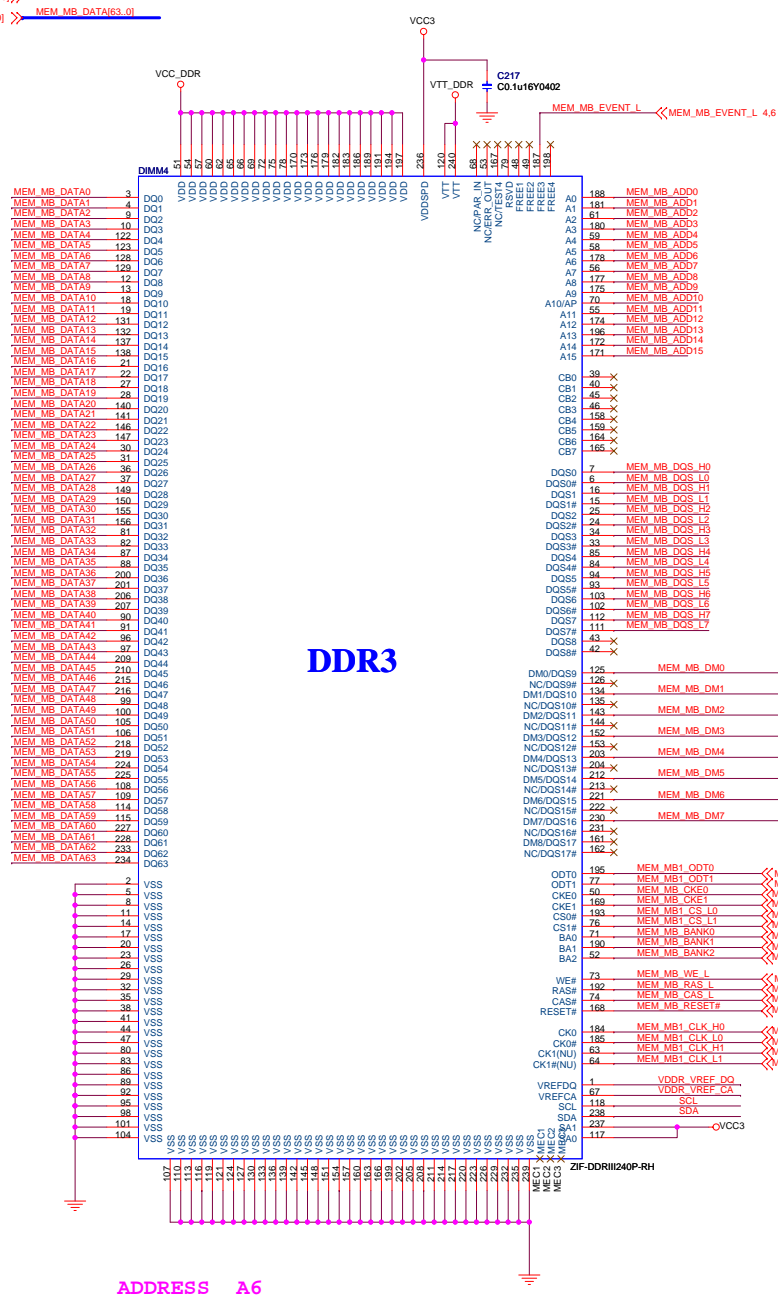


4.6 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
4.6 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
4.6 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
4.6 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
4.6 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]



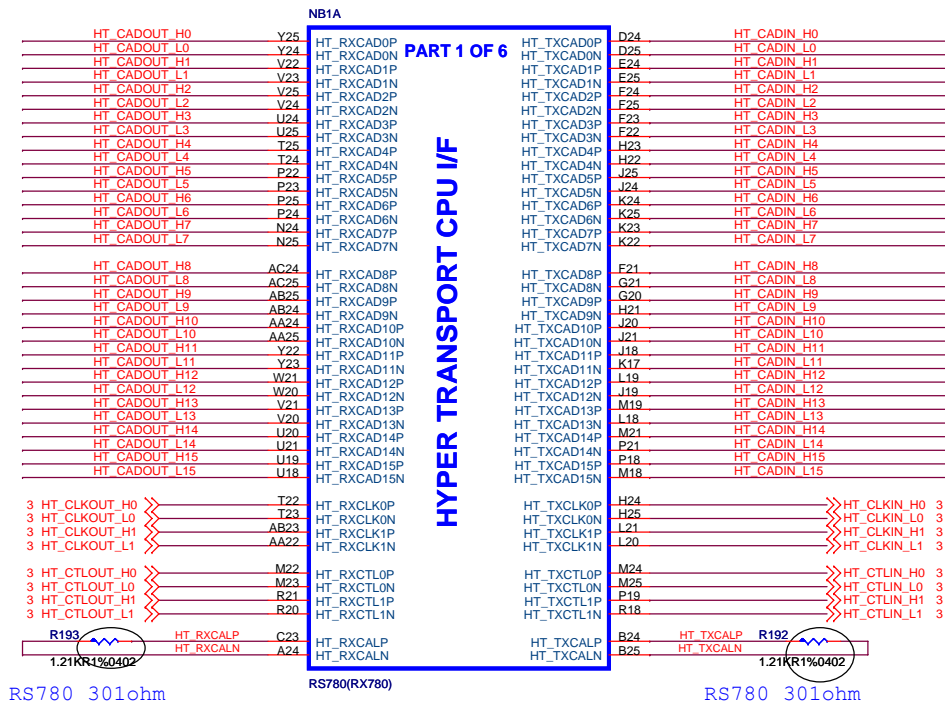
ADDRESS A4

4.6 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
4.6 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
4.6 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
4.6 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
4.6 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]



ADDRESS A6

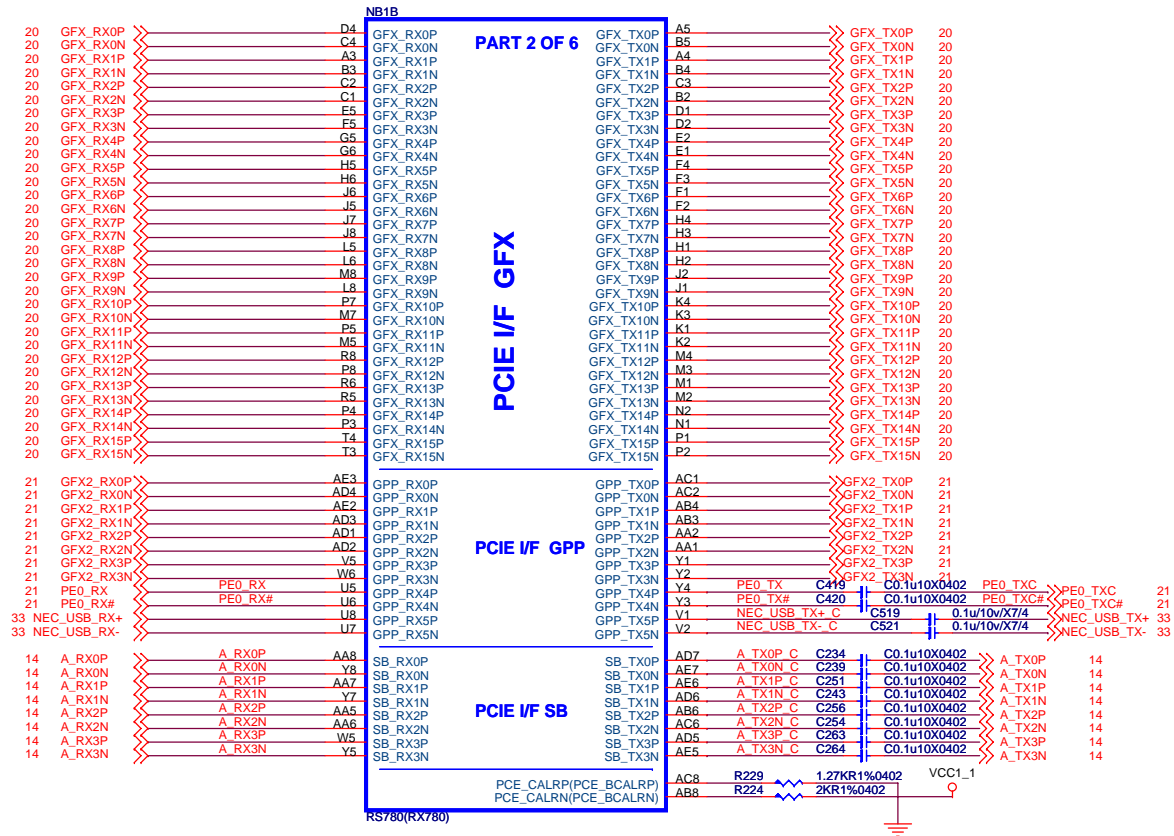
3 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
3 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
3 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
3 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]



RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			

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Title		Rev	
RD780-HT LINK I/F		4.0	
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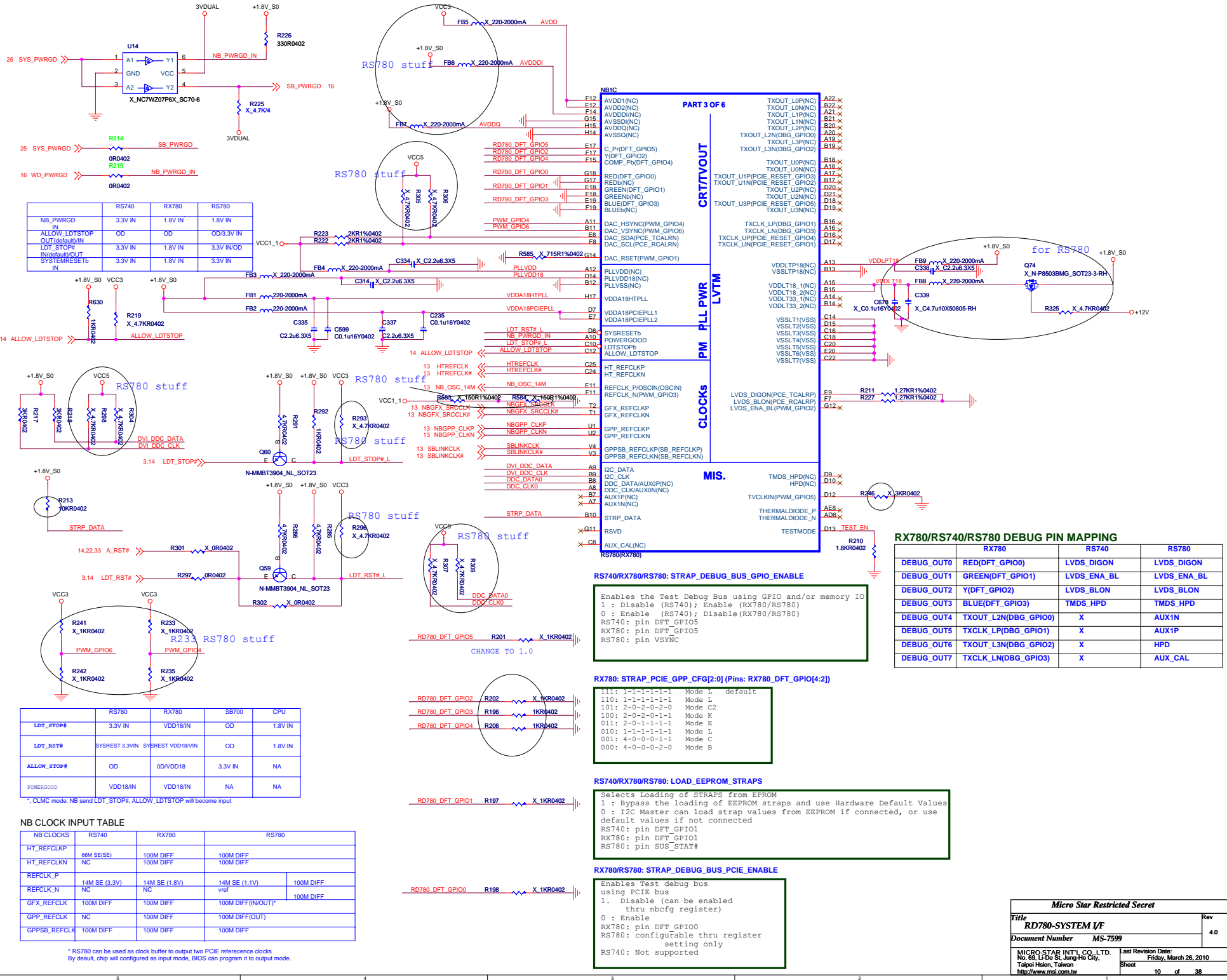


RX740/RS740/RS780 difference table (PCIE LINK)

	RS740	RX740/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLOK	LVDS_BLOK
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

	RS780	RX780	SB700	CPU
LDT_STOP#	3.3V IN	VDD18IN	OD	1.8V IN
LDT_RST#	SYSEST 3.3V IN	SYSEST VDD18/VIN	OD	1.8V IN
ALLOW_STOP#	OD	OD/VDD18	3.3V IN	NA
POWERGOOD	VDD18IN	VDD18IN	NA	NA

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

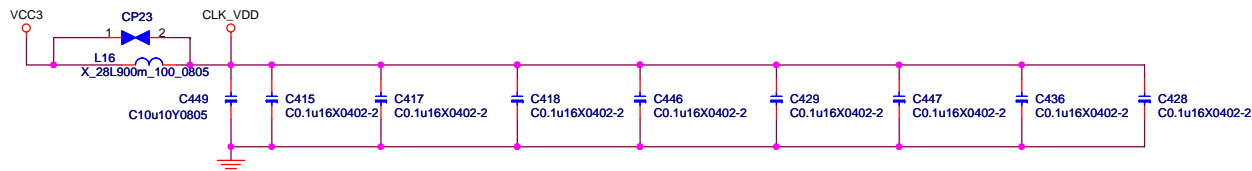
* CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP# will become input

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable (RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYN

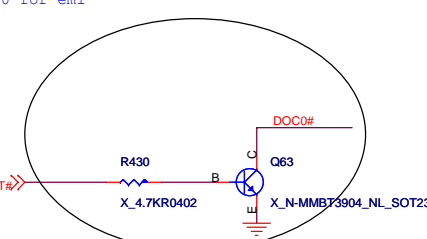
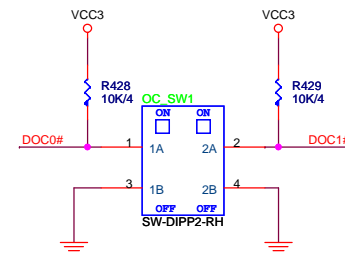
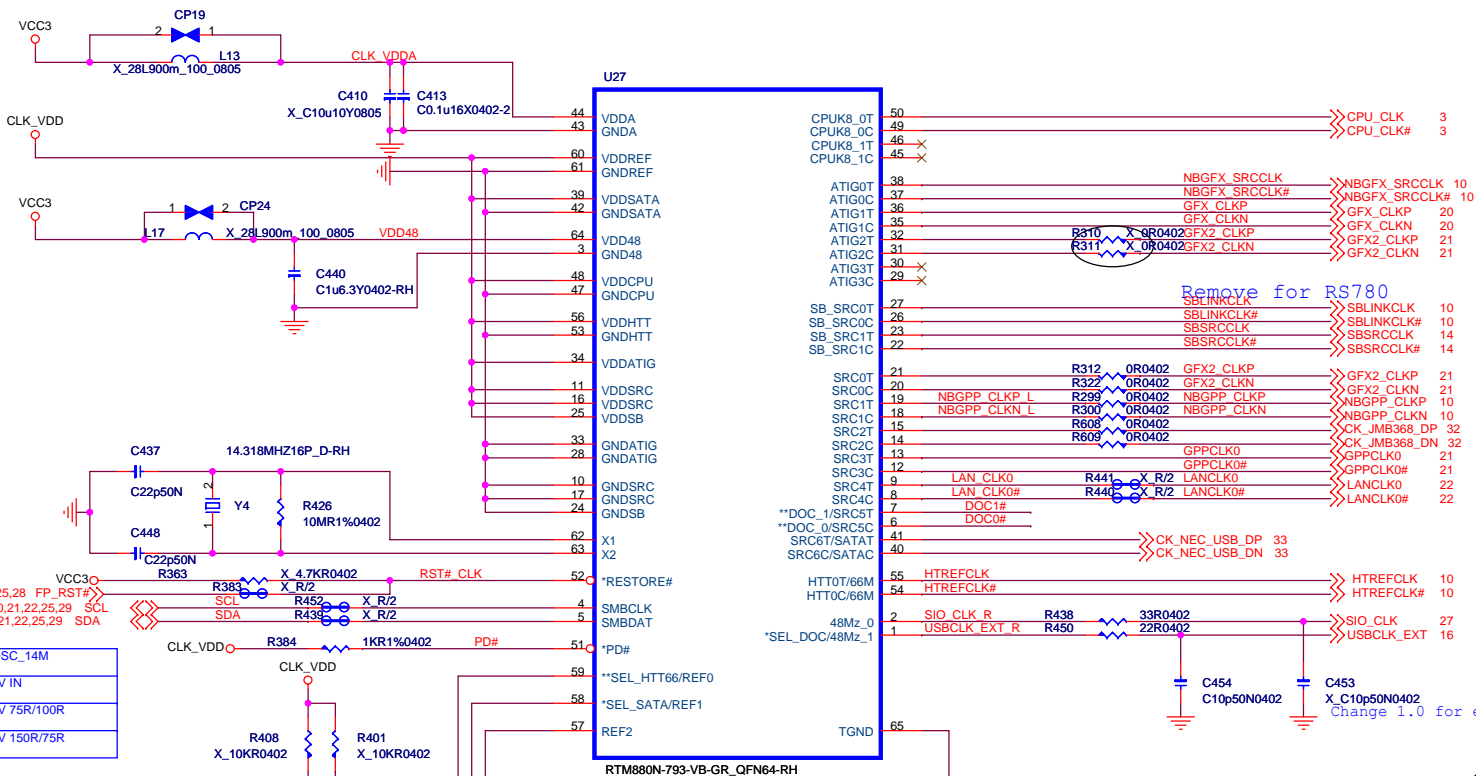
RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO(4:2))
111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B

RS740/RX780/RS780: LOAD_EEPROM_STRAPS
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE
Enables Test debug bus using PCIE bus
1. Disable (can be enabled thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register setting only
RS740: Not supported



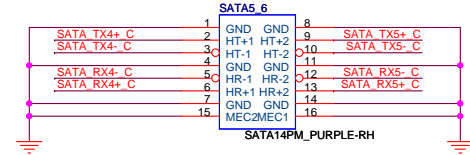
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U19 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U19 POWER PIN



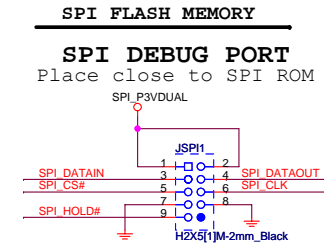
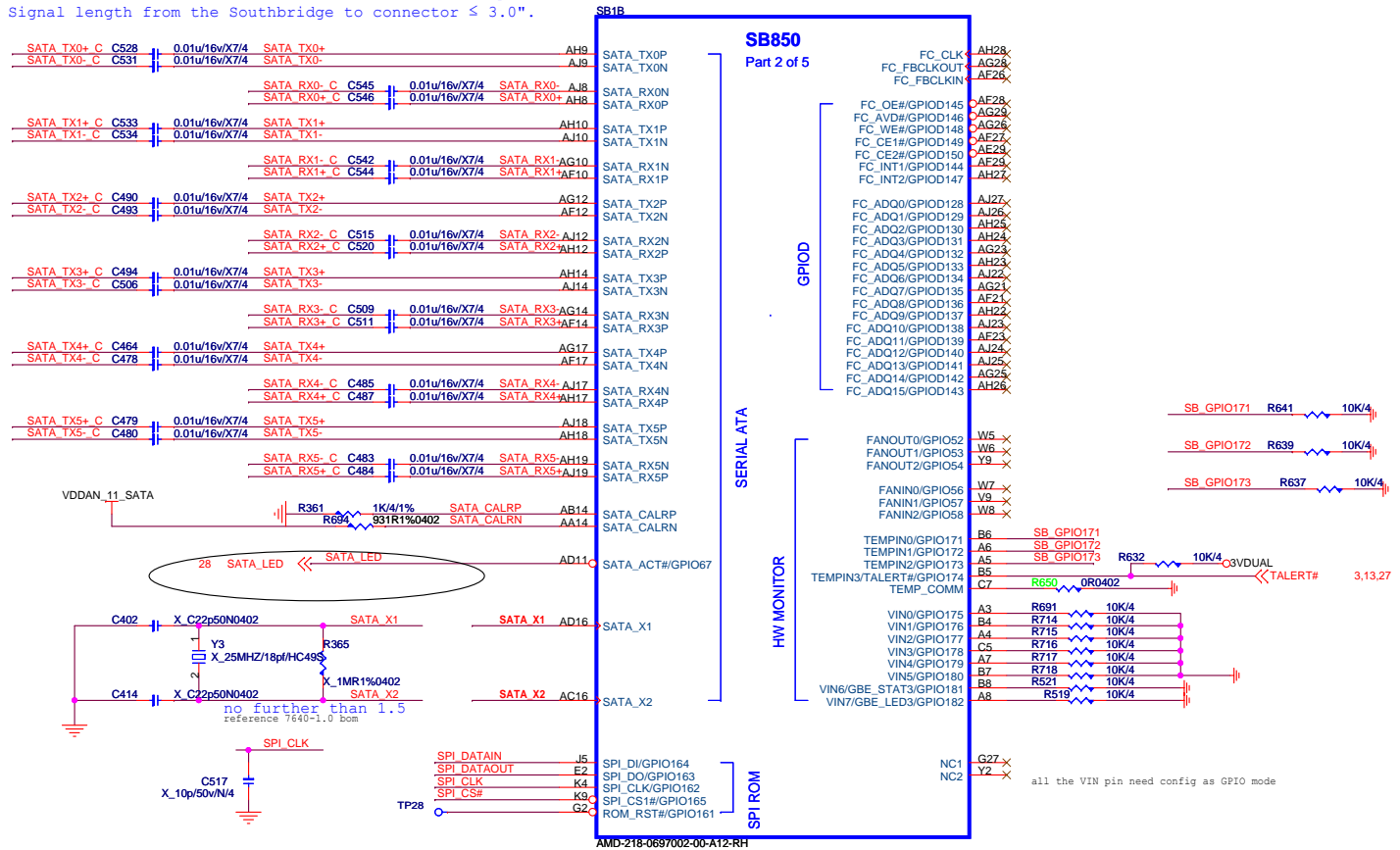
	NB_OSC_14M
RS740	3.3V IN
RX780	1.8V 75R/100R
RS780	1.1V 150R/75R

SEL_HTT66 : 'L' 100Mhz FOR 780
'H' 66Mhz FOR 740

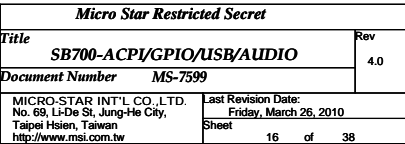
Micro Star Restricted Secret		
Title	Clock Generator RTM880N-793	Rev
Document Number	MS-7599	4.0
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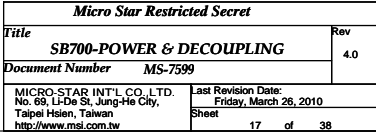


SATA_TX[5:0]P/N: Routed with 100-ohm \pm 10% differential impedance.
SATA_RX[5:0]P/N: Routed with 90-ohm \pm 10% differential impedance.
Gen3: Signal length from the Southbridge to connector \leq 3.0".



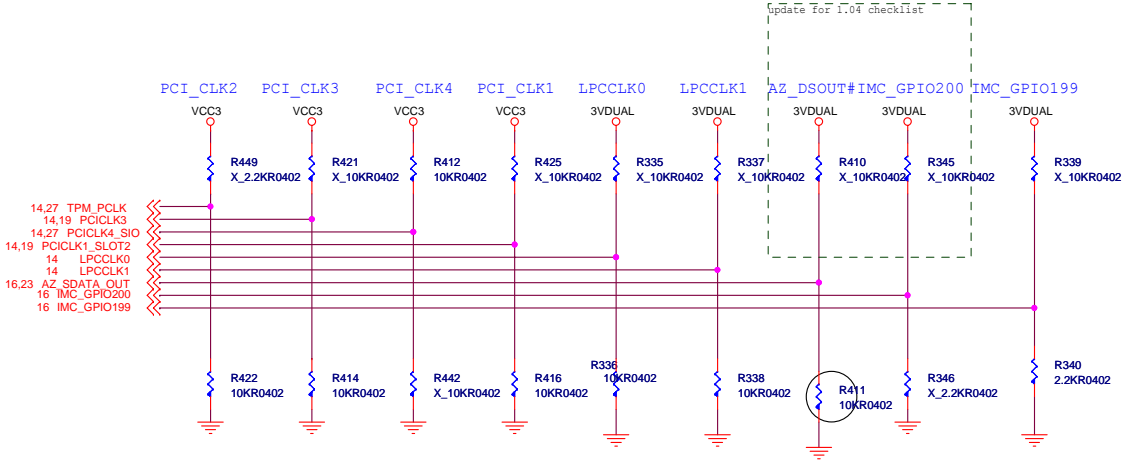
Part Number : N31-2051451-H06





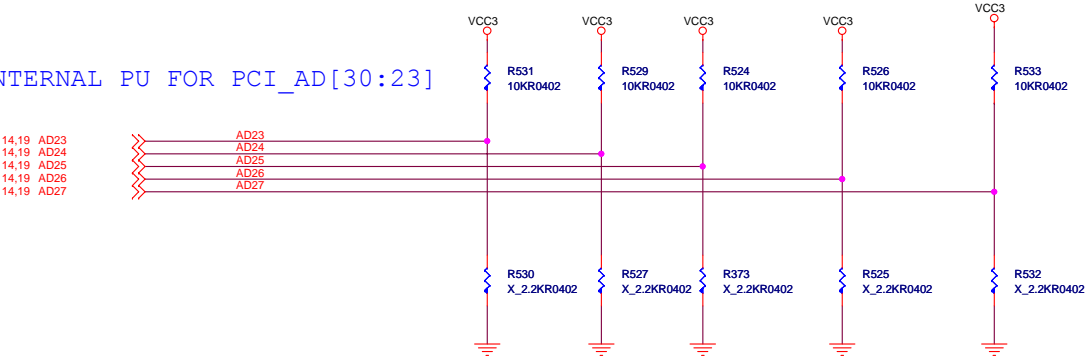
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



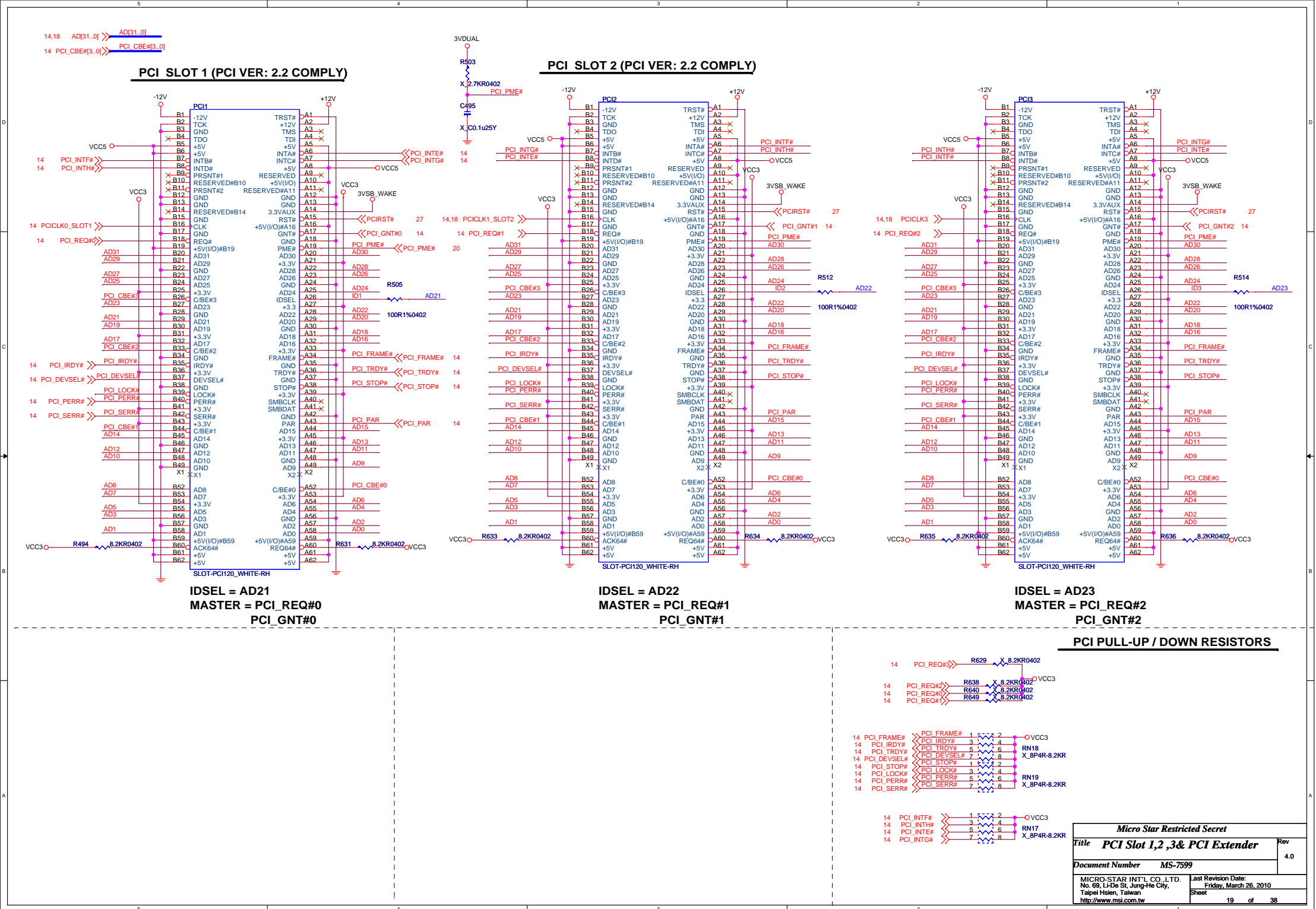
	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_DOUT#	IMC_GPIO200	IMC_GPIO199
PULL HIGH	ALLOW PCIE GEN2	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE DEFAULT	UEC ENABLE	CLKGEN ENABLED		ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE	DISABLE EC DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	L, H = LPC ROM L, L = FWH ROM	

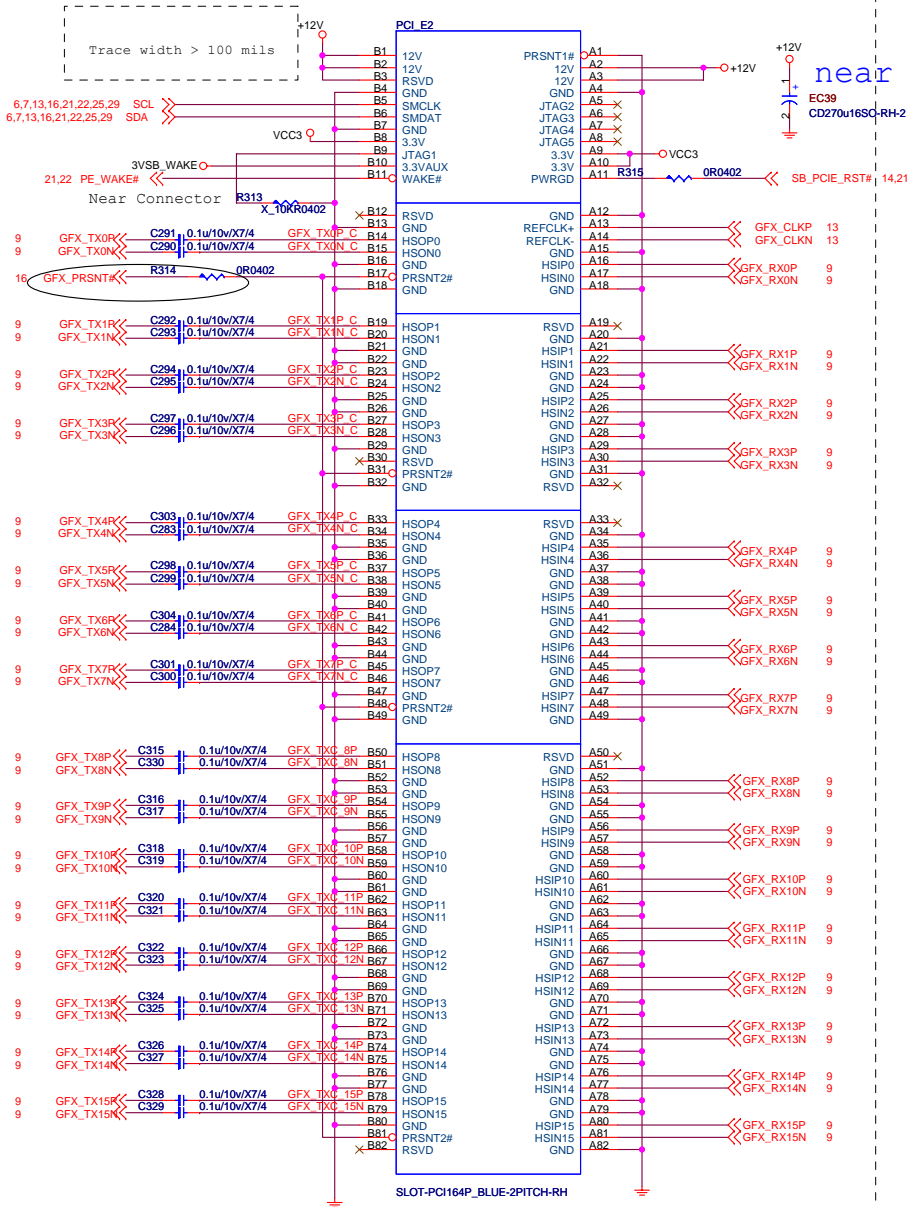
SB800 HAS 15K INTERNAL PU FOR PCI_AD[30:23]



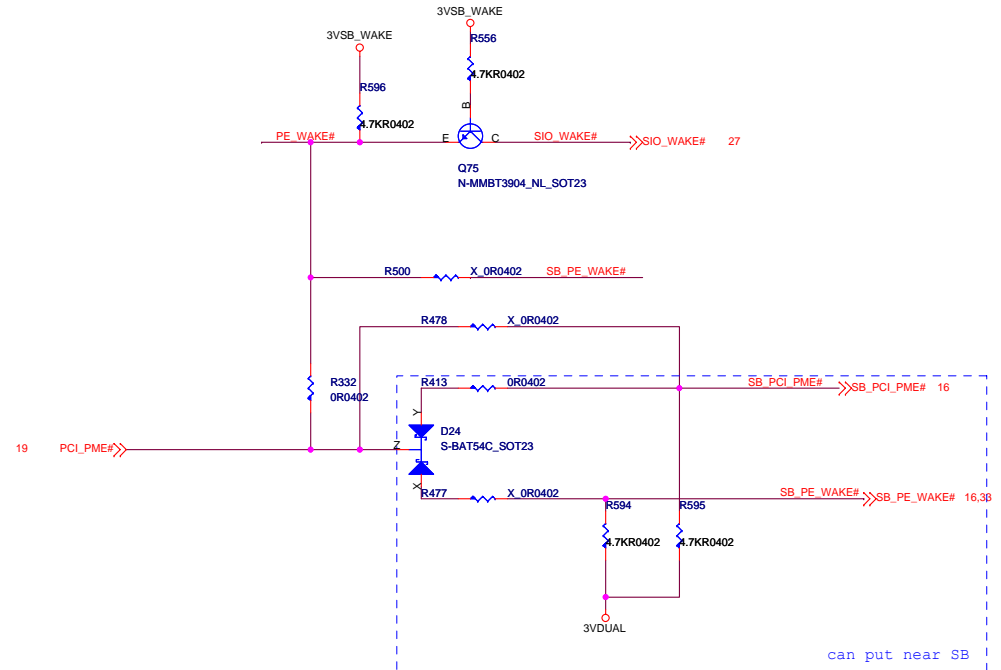
DEBUG STRAPS

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



PCI EXPRESS_16

near PCIE X16 Slot



Digital Switch	
SEL pin	SLI function

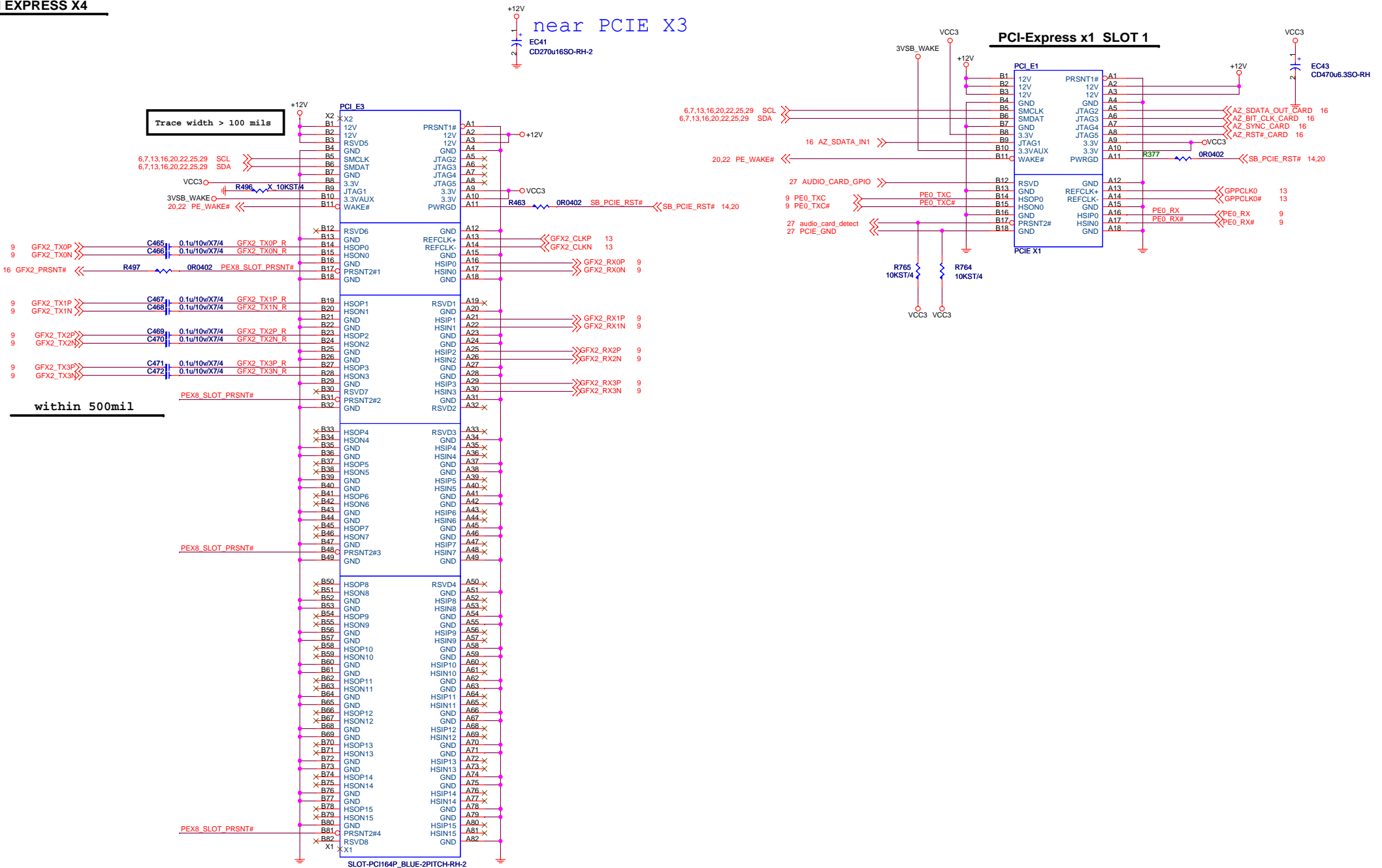
SEL (X8 X8#)	Output	X8 SW	PCI-E Slot 1/2
Low	Oa	Low	X8 / X8
Hi	Ob	Hi	X16 / 0

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Title	Rev
<i>PCI-E X16 , X1 Slot</i>	4.0
Document Number <i>MS-7599</i>	

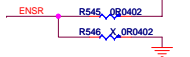
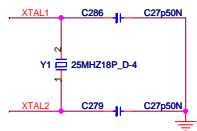
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PCI EXPRESS X4

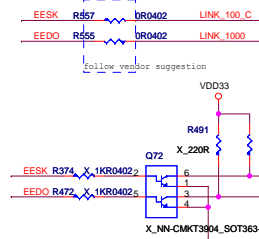


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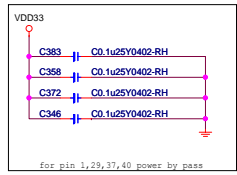
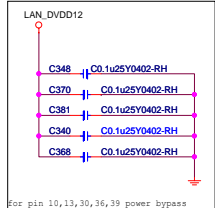
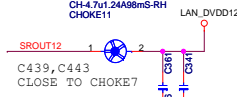
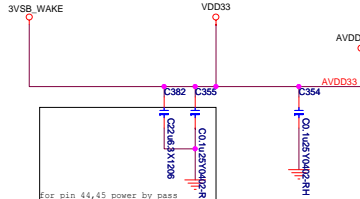
Title <i>PCIE X1 Slot 1, 2</i>		Rev 4.0
Document Number <i>MS-7599</i>		
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High:Enable SW on LAN
Low:Disable SW on LAN

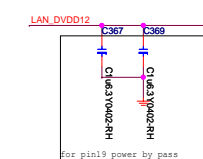
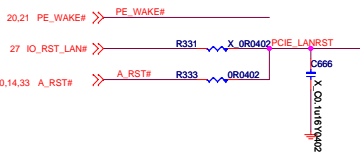
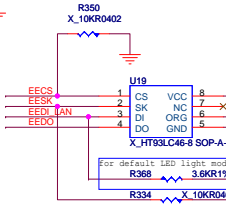
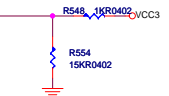
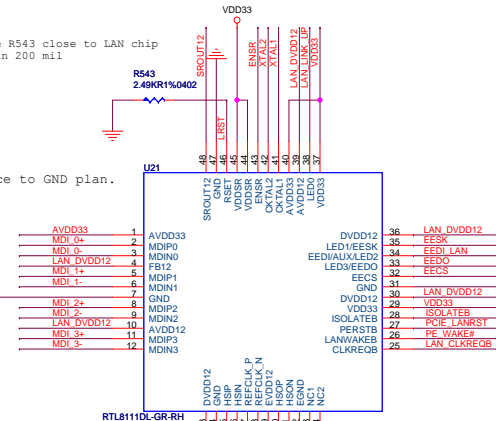


Follow vendor suggestion



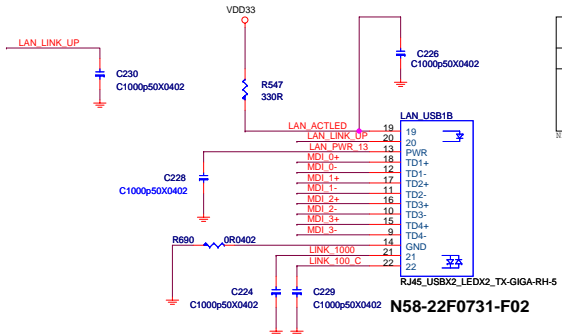
Place R543 close to LAN chip within 200 mil

MDix+/- Reference to GND plan.



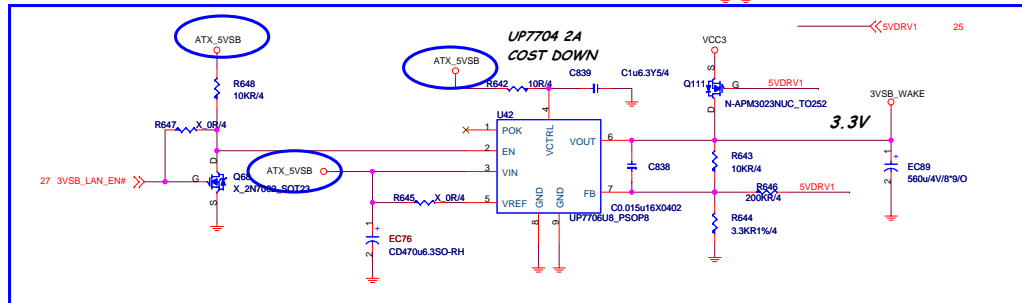
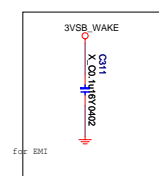
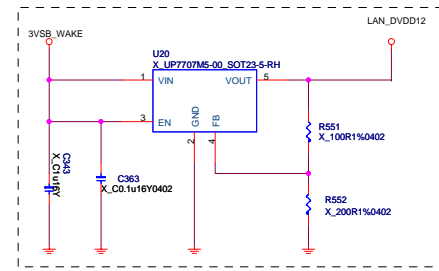
Power domain chart

	RTL8111DL
AVDD33	3.3V
VDDSR	3.3V
VDD33	3.3V
EVDD12	1.2V
DVDD12	1.2V
AVDD12	1.2V

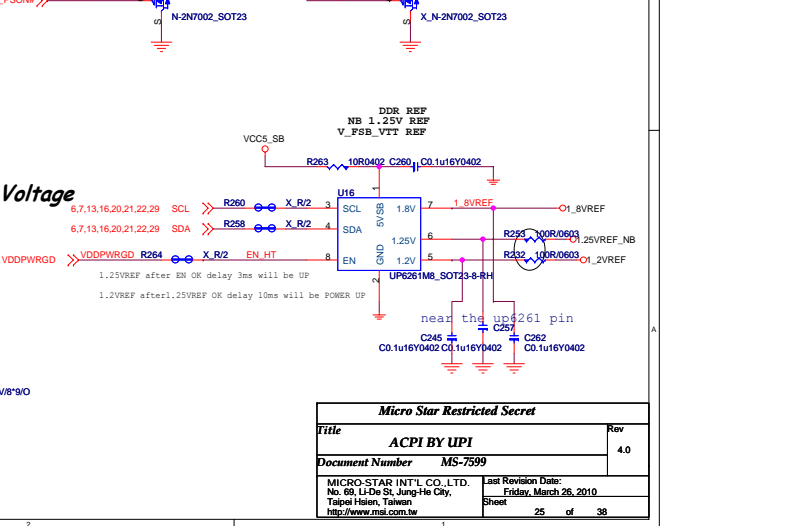
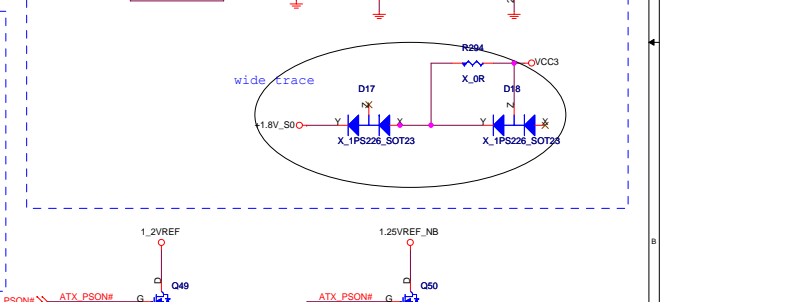
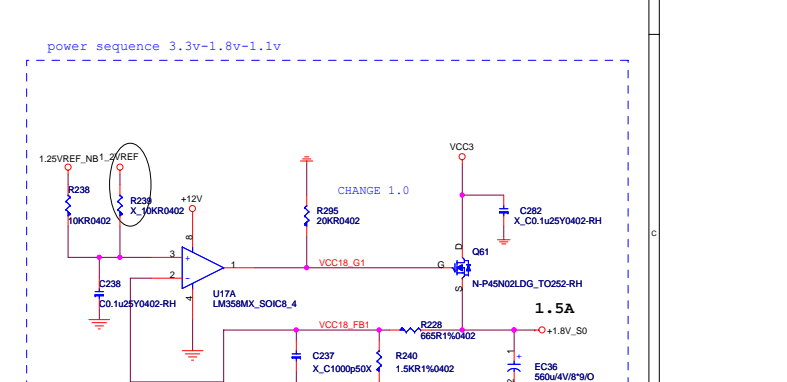
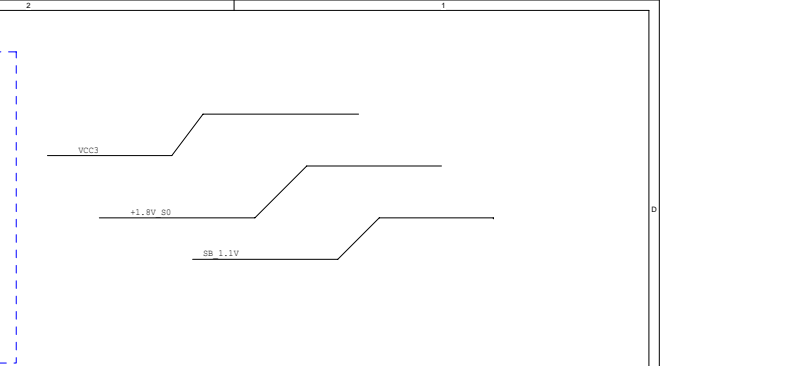
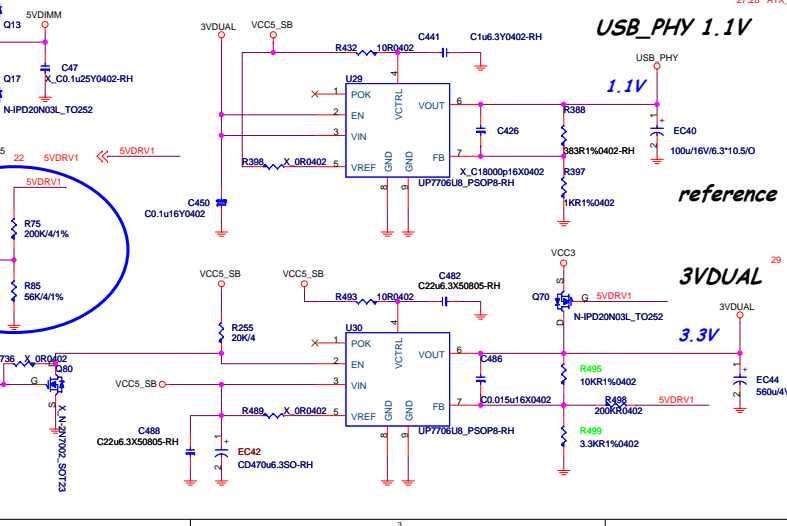
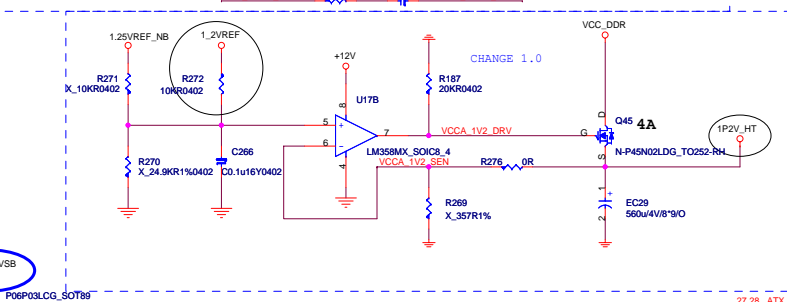
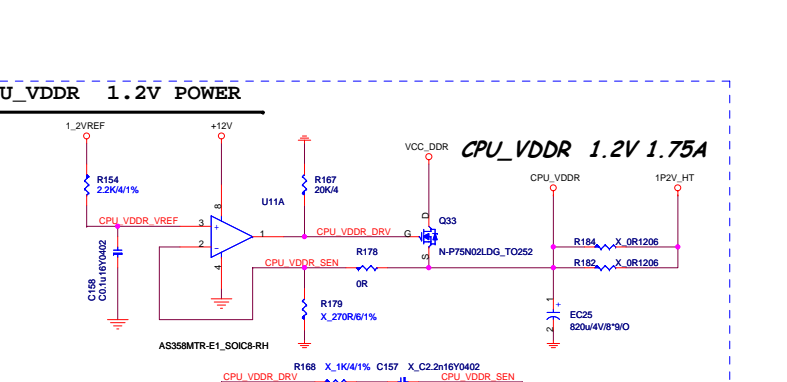
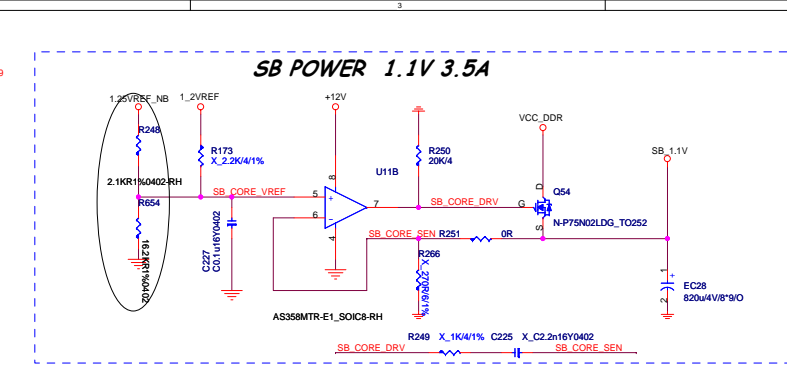
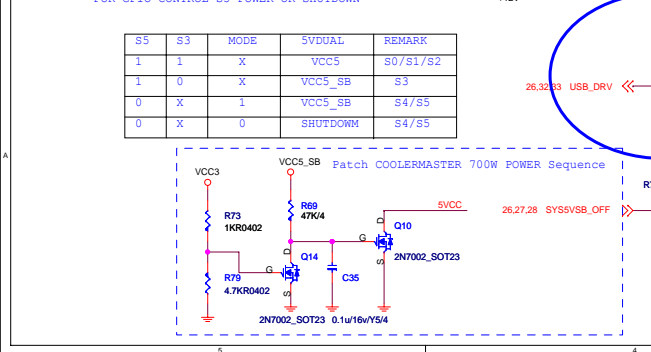
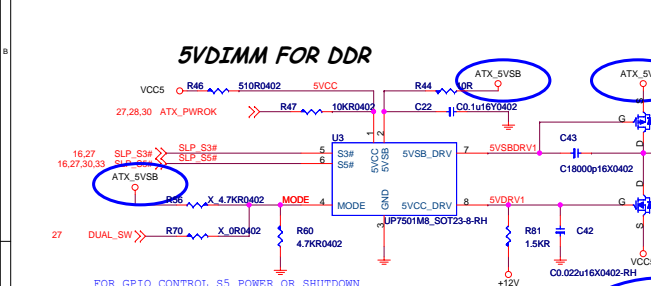
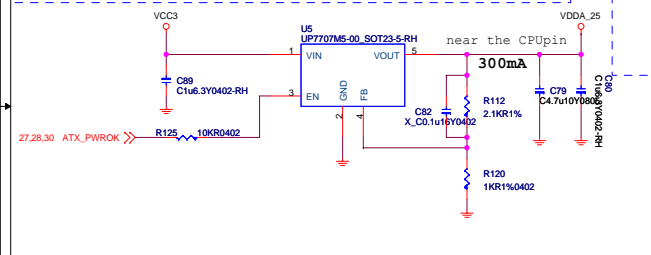
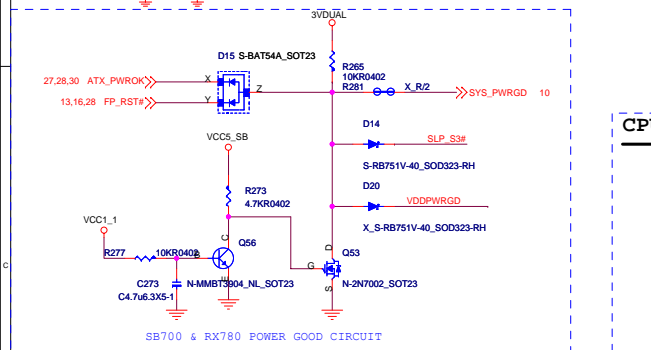
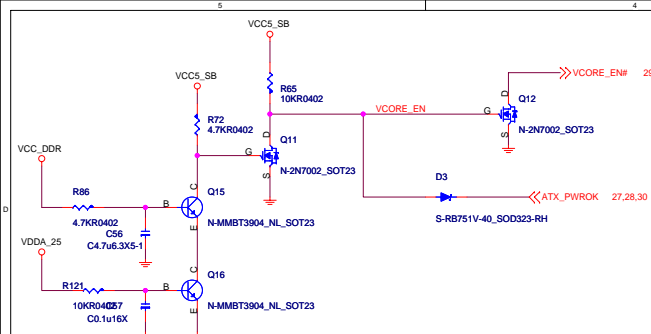


Power consumption			
	1G	100M	
3.3V	103mA	TBD	
1.5V	367mA	TBD	
1.8V	198mA	TBD	

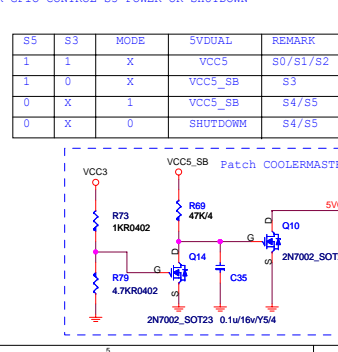
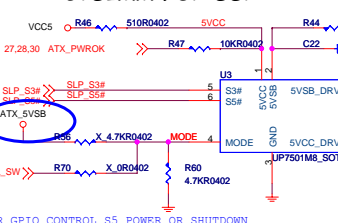
Giga-Lan		10/100-Lan	
N58-22F0081-642	N58-22F0061-642	N58-22F0061-P02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19	Yellow	19	Yellow
20	Yellow	20	Yellow
21	Orange	21	Orange
22	Green	22	Green



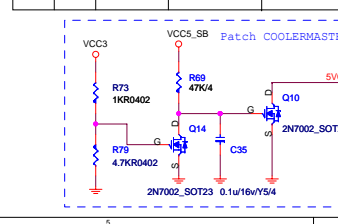
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Document Number	MS-7599	
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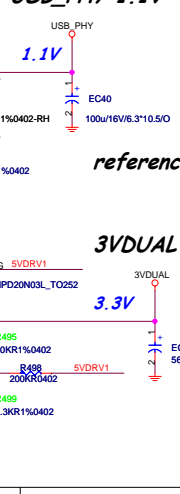
5VDDIMM FOR DDR



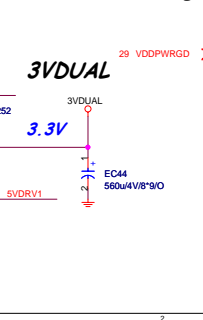
S5	S3	MODE	5VDDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWN	S4/S5



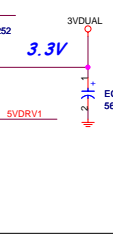
USB_PHY 1.1V



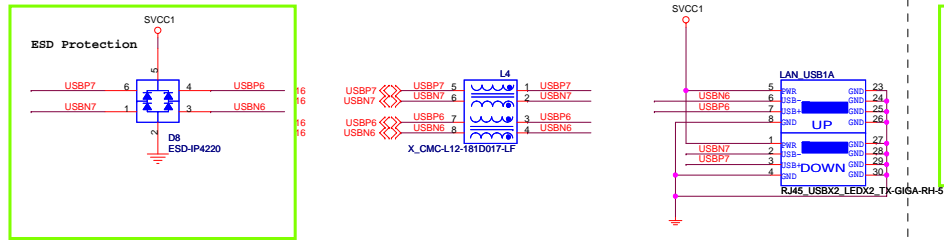
reference Voltage



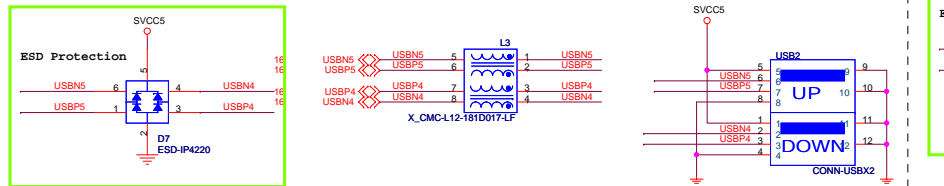
3VDDUAL



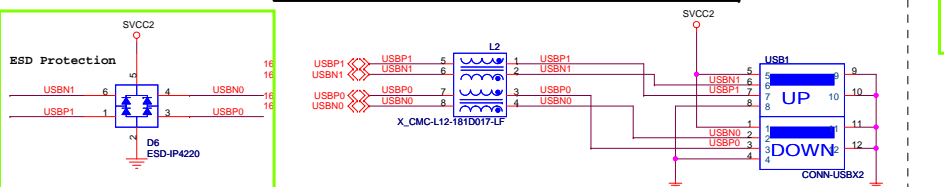
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



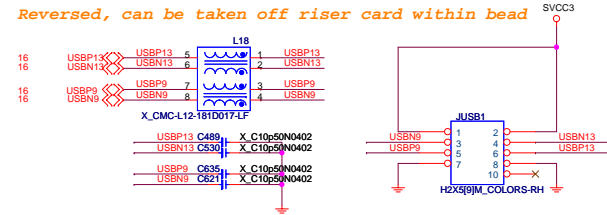
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



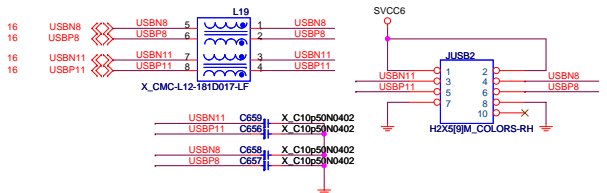
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



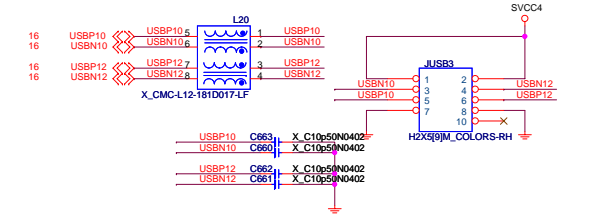
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



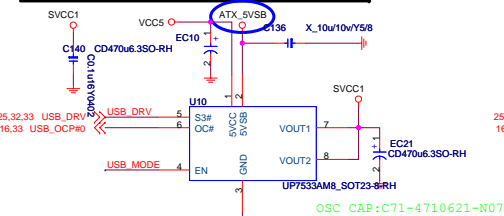
FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



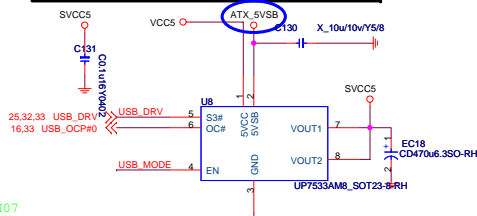
FRONT PANEL USB CONNECTOR FOR USB PORT 10,11



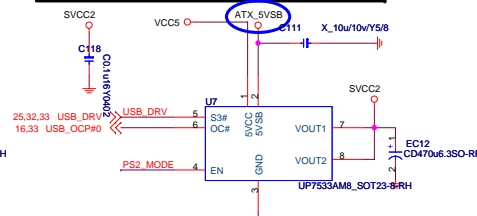
POWER CIRCUIT FOR USB PORT 0,1



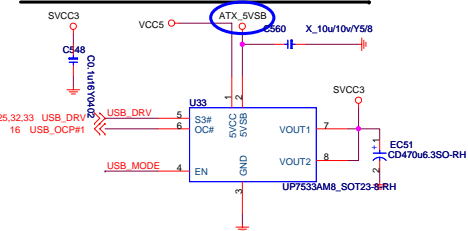
POWER CIRCUIT FOR USB PORT 2,3



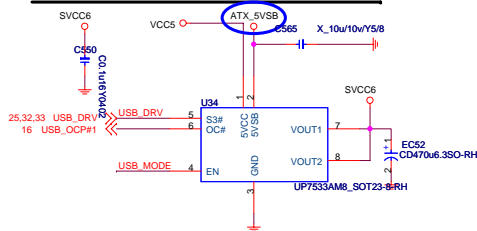
POWER CIRCUIT FOR USB PORT 4,5



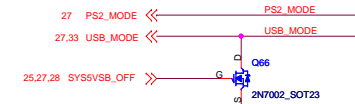
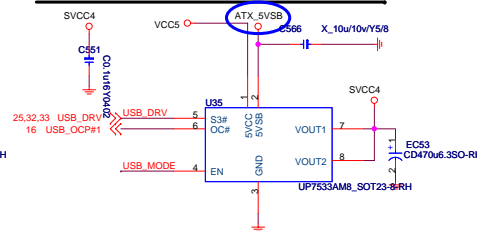
POWER CIRCUIT FOR USB PORT 6,7



POWER CIRCUIT FOR USB PORT 8,9



POWER CIRCUIT FOR USB PORT 10,11



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LPC SUPER I/O F71889

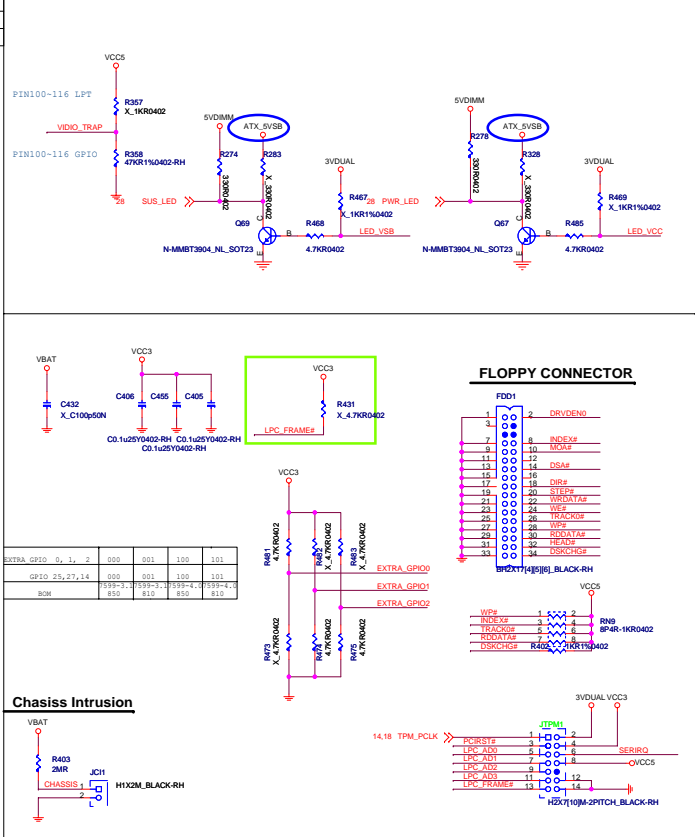
[illegible]

Figure 1: Thermal Resistor Schematic Diagram. This diagram illustrates the electrical connections for the thermal resistor (R369) and the status panel. It includes connections for VBAT, R403, JCH1, CHASSIS, HX2M_BLACK-RH, 14.18 TPM_PCLK, PCORESYS, LPU_AIO0, LPU_AIO1, LPU_AIO2, LPU_AIO3, LPU_PROXDEF, SERIO0, VCC5, HX2V10M-3PITCH_BLACK-RH, R366, R367, R365, R372, R375, R379, R378, R377, R376, R375, R374, R373, R372, R371, R370, R369, R368, R367, R366, R365, R364, R363, R362, R361, R360, R359, R358, R357, R356, R355, R354, R353, R352, R351, R350, R349, R348, R347, R346, R345, R344, R343, R342, R341, R340, R339, R338, R337, R336, R335, R334, R333, R332, R331, R330, R329, R328, R327, R326, R325, R324, R323, R322, R321, R320, R319, R318, R317, R316, R315, R314, R313, R312, R311, R310, R309, R308, R307, R306, R305, R304, R303, R302, R301, R300, R299, R298, R297, R296, R295, R294, R293, R292, R291, R290, R289, R288, R287, R286, R285, R284, R283, R282, R281, R280, R279, R278, R277, R276, R275, R274, R273, R272, R271, R270, R269, R268, R267, R266, R265, R264, R263, R262, R261, R260, R259, R258, R257, R256, R255, R254, R253, R252, R251, R250, R249, R248, R247, R246, R245, R244, R243, R242, R241, R240, R239, R238, R237, R236, R235, R234, R233, R232, R231, R230, R229, R228, R227, R226, R225, R224, R223, R222, R221, R220, R219, R218, R217, R216, R215, R214, R213, R212, R211, R210, R209, R208, R207, R206, R205, R204, R203, R202, R201, R200, R199, R198, R197, R196, R195, R194, R193, R192, R191, R190, R189, R188, R187, R186, R185, R184, R183, R182, R181, R180, R179, R178, R177, R176, R175, R174, R173, R172, R171, R170, R169, R168, R167, R166, R165, R164, R163, R162, R161, R160, R159, R158, R157, R156, R155, R154, R153, R152, R151, R150, R149, R148, R147, R146, R145, R144, R143, R142, R141, R140, R139, R138, R137, R136, R135, R134, R133, R132, R131, R130, R129, R128, R127, R126, R125, R124, R123, R122, R121, R120, R119, R118, R117, R116, R115, R114, R113, R112, R111, R110, R109, R108, R107, R106, R105, R104, R103, R102, R101, R100, R99, R98, R97, R96, R95, R94, R93, R92, R91, R90, R89, R88, R87, R86, R85, R84, R83, R82, R81, R80, R79, R78, R77, R76, R75, R74, R73, R72, R71, R70, R69, R68, R67, R66, R65, R64, R63, R62, R61, R60, R59, R58, R57, R56, R55, R54, R53, R52, R51, R50, R49, R48, R47, R46, R45, R44, R43, R42, R41, R40, R39, R38, R37, R36, R35, R34, R33, R32, R31, R30, R29, R28, R27, R26, R25, R24, R23, R22, R21, R20, R19, R18, R17, R16, R15, R14, R13, R12, R11, R10, R9, R8, R7, R6, R5, R4, R3, R2, R1, R0.

DRIVE

A B C D E F

C VCCS

W-ROTOR-16STEPS-RH-1

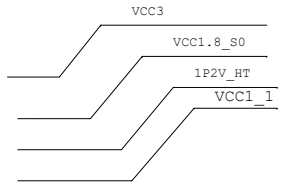
die display text

Intel Front Panel

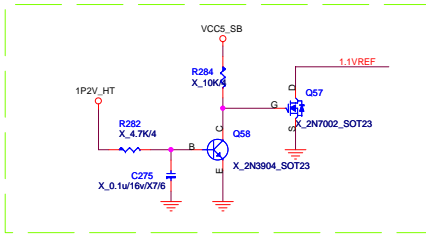


Title		Rev 4.0
ATX connector / Front Panel/KB		
Document Number MS-7599		
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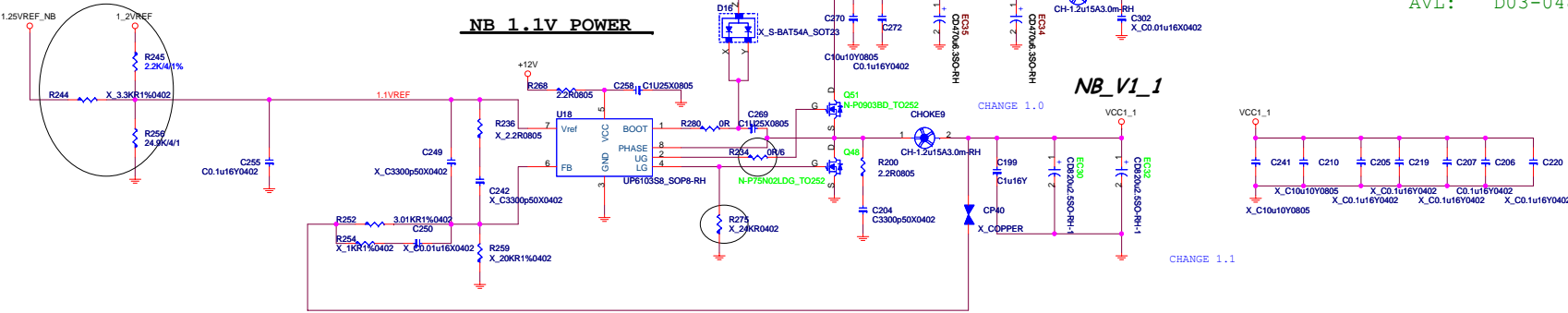
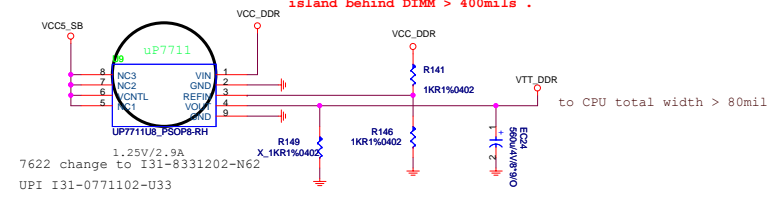
RX780 power up sequence



Reserve for RX780 POS

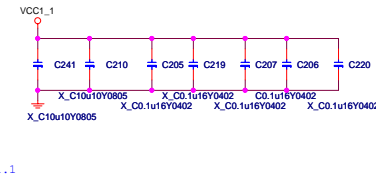


DDR VTT Power

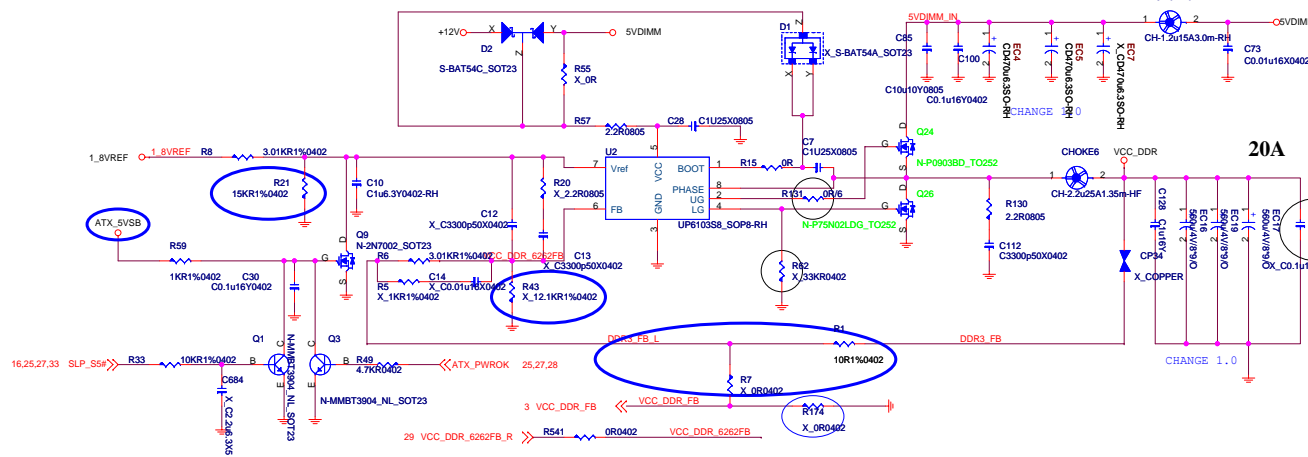


H-MOS: D03-0903BDB-N03
AVL: D03-0480900-O05
L-MOS: D03-75N022B-N03
AVL: D03-0480600-O05

NB_V1_1



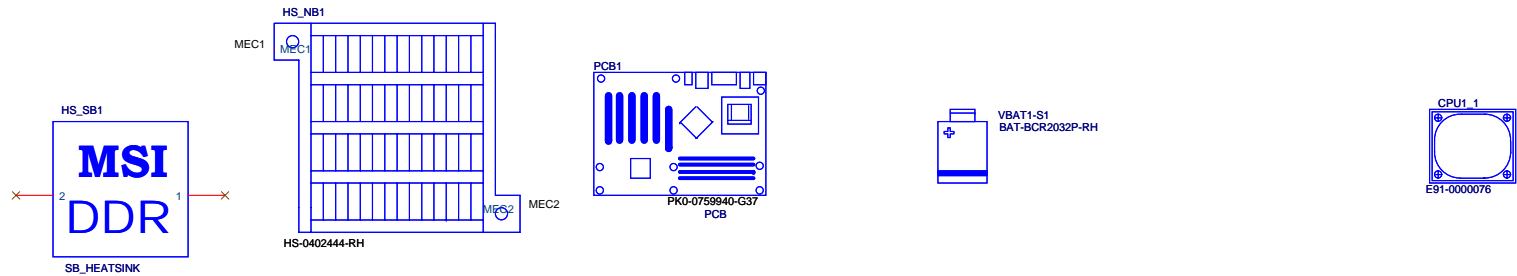
DDR III 1.5V POWER



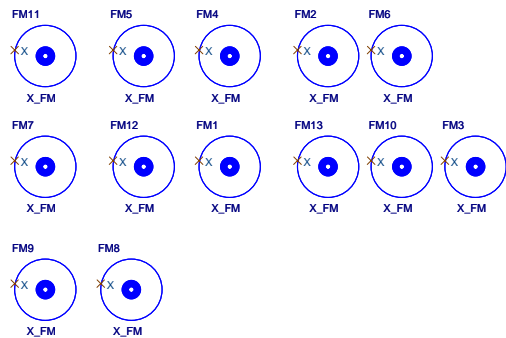
VCC_DDR

20A

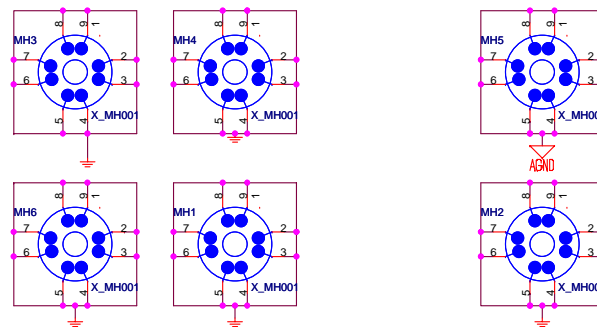
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Document Number	MS-7599	
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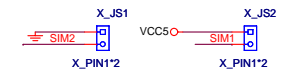
Optics Orientation Holes



Mounting Holes



Simulation



Micro Star Restricted Secret		
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